OIPE JC104
APR 05 2005
PATENT & TRADEMARK OFFICE

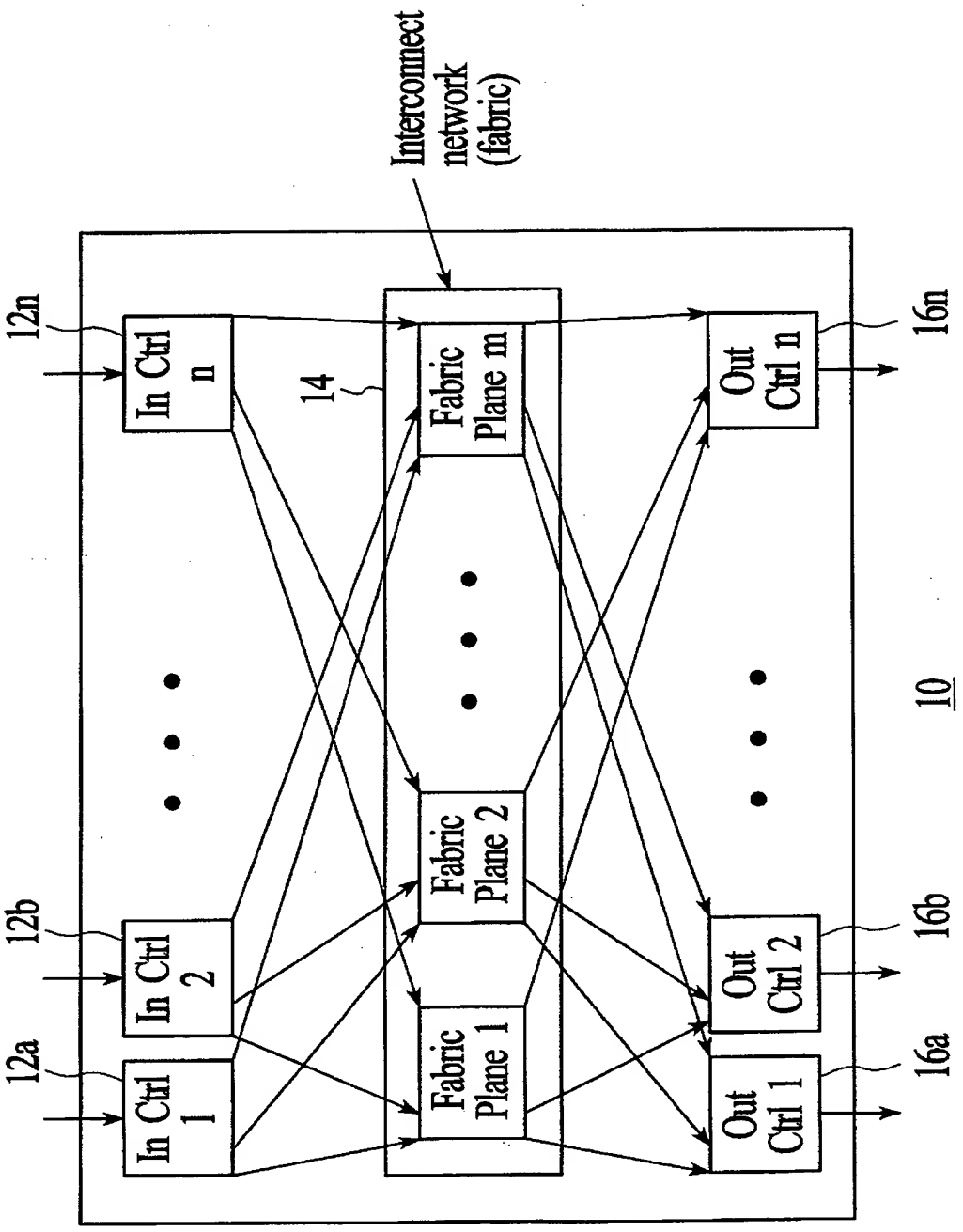


FIG. 1

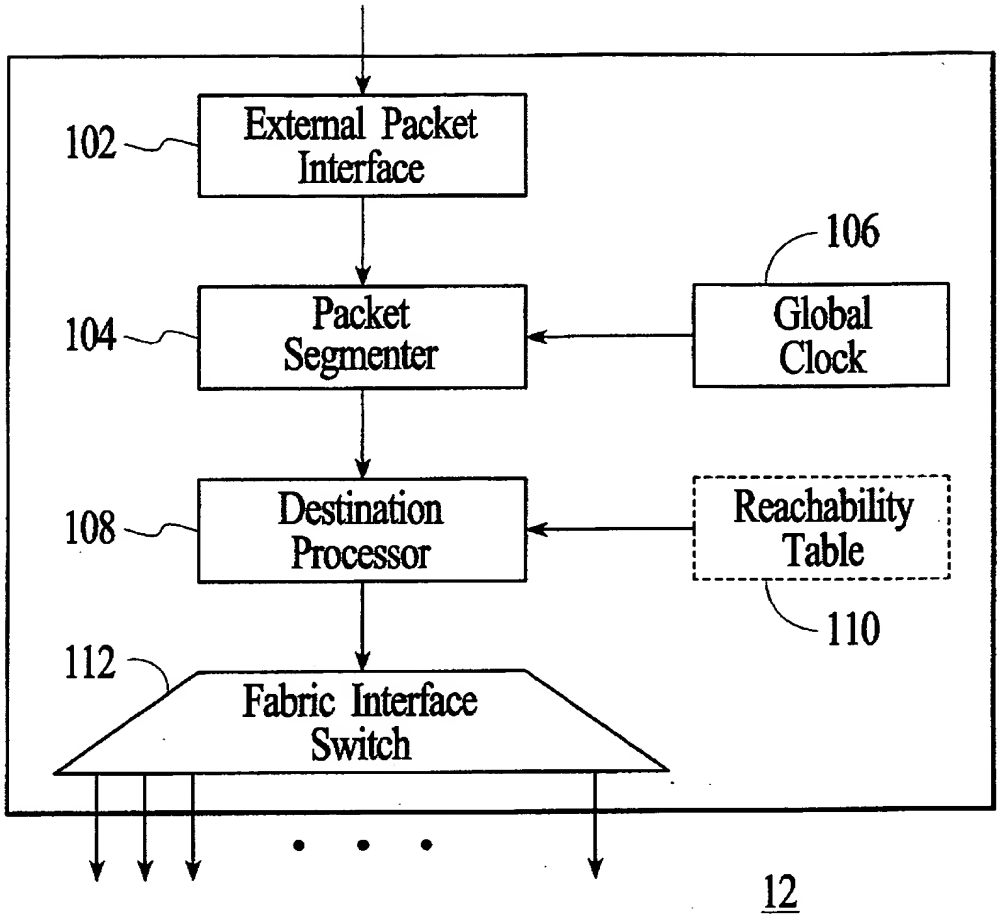


FIG. 2

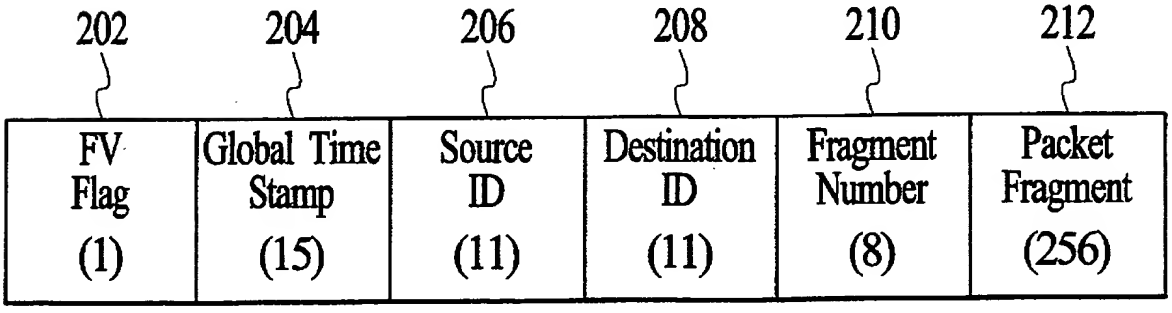


FIG. 3 200

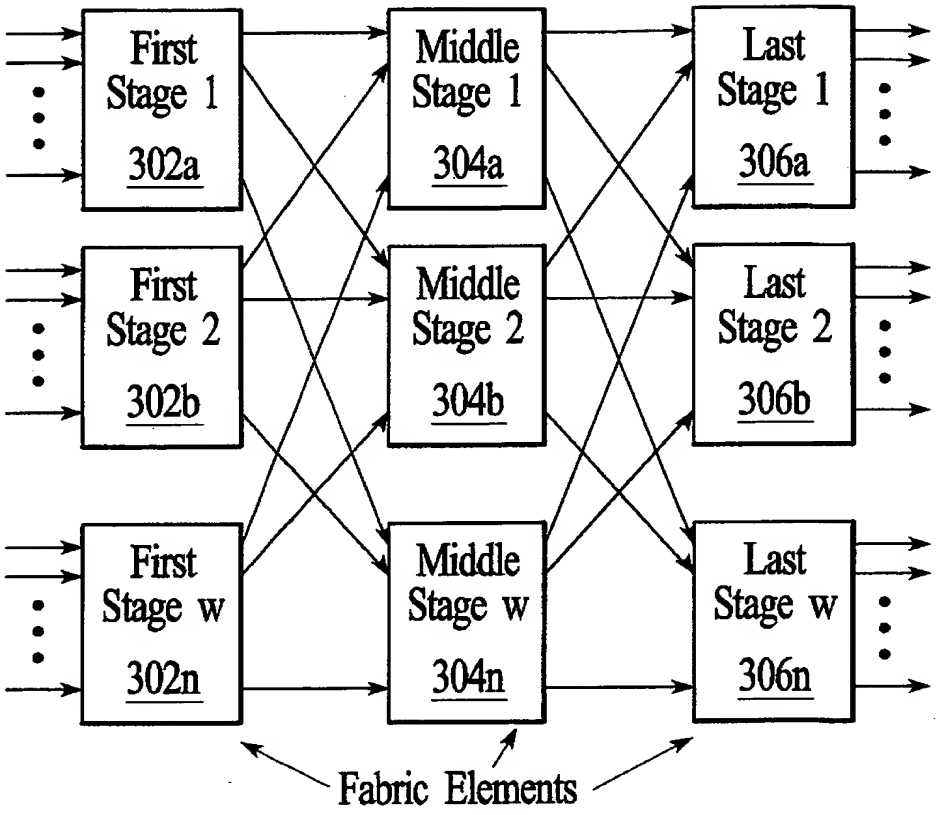


FIG. 4

14

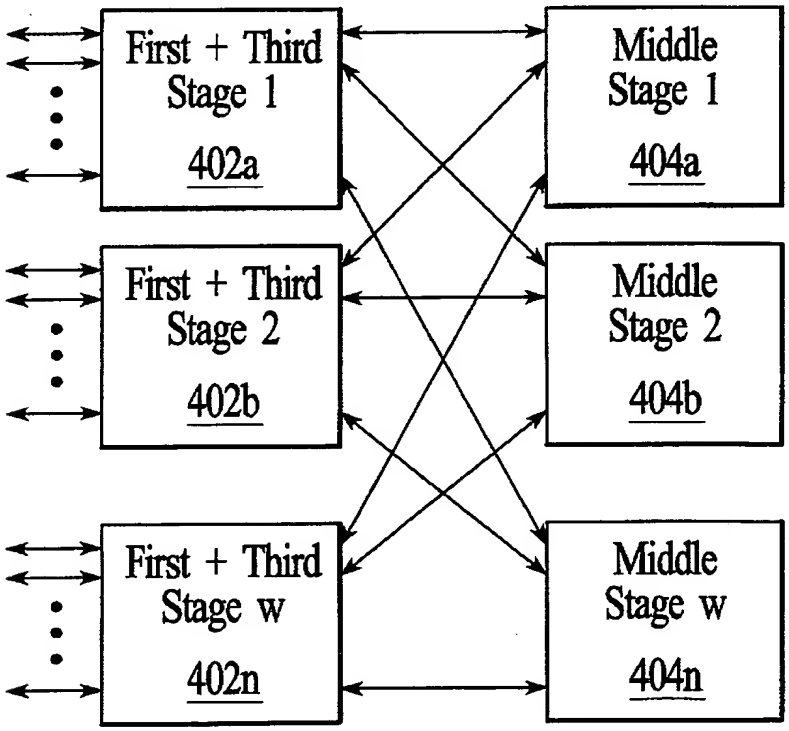


FIG. 4A

400

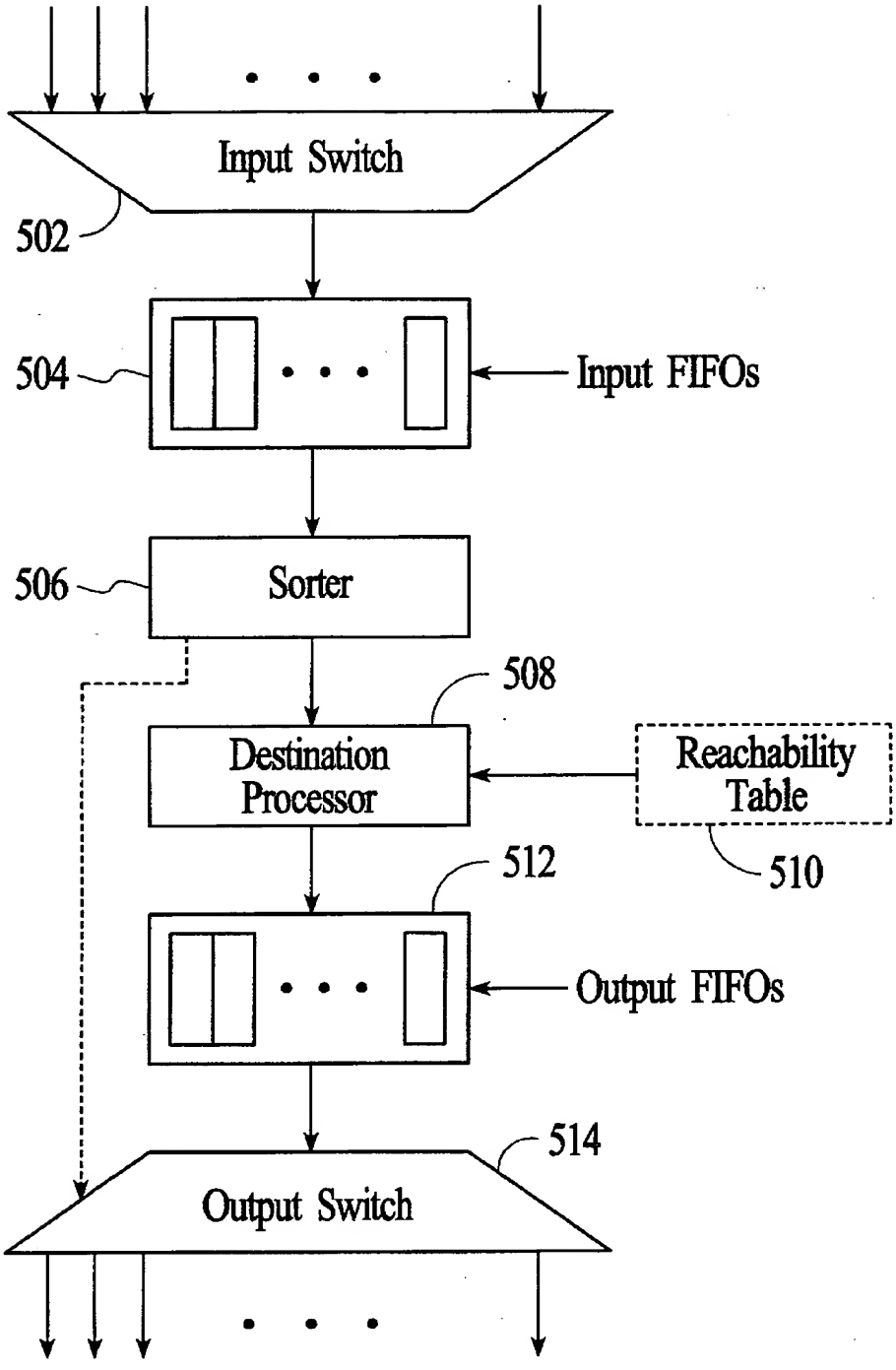
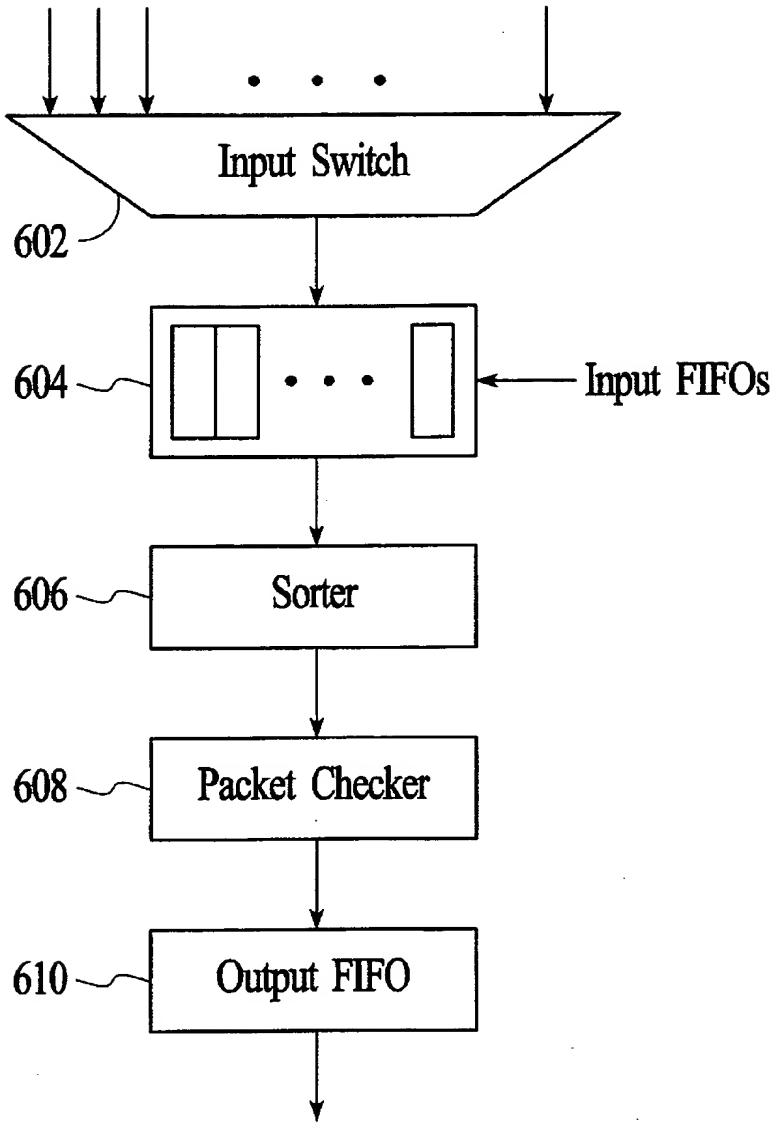

Input Switch
502
504
Input FIFOs
506
Sorter
508
Destination Processor
Reachability Table
510
512
Output FIFOs
514
Output Switch
500

FIG. 5


Input Switch
602
604
Input FIFOs
606
Sorter
608
Packet Checker
610
Output FIFO

16

FIG. 6